CLAIMS:

A method of forming a semiconductor structure comprising a substrate having a patterned ONO insulating layer over a portion thereof, and characterized by the steps of forming an insulating layer comprising an Oxide-Nitride-Silicon layered structure on the substrate, applying a photoresist to the silicon surface as part of a patterning process and stripping the photoresist once a required patterning step has been completed, and subsequently re-oxidizing the silicon layer of the remaining Oxide-Nitride-Silicon structure so as to form an ONO insulating layer structure.

2. A method as claimed in claim 1, wherein the silicon layer comprises an amorphous silicon layer.

3. A method as claimed in claim 1 or 2, wherein a non-volatile memory cell is applied as part of the semiconductor structure, which non-volatile memory cell employs the ONO insulating layer between a floating gate and control gate thereof.

4. A method as claimed in claim 3, wherein the non-volatile memory cell is applied with a control gate formed from a conductive layer which also serves to form part of a peripheral semiconductor structure.

5. A method as claimed in claim 1, 2, 3 or 4, wherein the subsequent oxidation of the silicon sub-layer of the Oxide-Nitride-Silicon insulating layer takes place also to provide a high voltage oxide layer for a peripheral structure.

6. A method as claimed in any one of claims 1 to 5, wherein the silicon layer is re-oxidized into a thermal oxide.